IEEE EDS Mini Colloquium on Semiconductor Electronics: Global Opportunity for the Americas

All time in EST (Virtual Meeting)
Each talk will be 25 minutes followed by 5 mins of Q&A
Date and time: 7th June, 2024. 10 am to 2 pm (EST)
Meeting link: https://purdue-edu.zoom.us/j/99313831210.org

EDS virtual colloquium on the future of CMOS technology, bringing together researchers from both North America and Latin America. The colloquium aims to explore emerging trends, challenges, and opportunities in CMOS technology, with a focus on potential collaborations between researchers in different regions.

Time (EST)	Speaker	Affiliation	Title/Topic
9:55 am	Dr. Jacobus Swart		Welcome message
10:00 am	Prof. Sayeef Salahuddin	EECS, U. California Berkeley	Energy Efficient AI Electronics
10:30 am	Dr. Felix Palumbo	UTN, Argentina	Spatio-Temporal Defect Generation Process in Irradiated HfO_2 MOS Stacks
11:00 am	Prof. Muhammad Hussain	ECE, Purdue University	Advanced Packaging and Heterogeneous Integration of 3D-IC
11:30 am	Prof. Gilson Wirth	Federal University of Rio Grande do Sul – UFRGS, Brazil	Charge Trapping Phenomena in Nanoscale Semiconductor Devices, including MOSFETS and Resistive Switching Memory
12:00 pm	Sr. Mgr. Katy Crist	Strategic Alliances & Partnerships, TEL	Semiconductor Workforce Development
12:30 pm	Dr. Edmundo A. Gutierrez	INAOE, Mexico	Research, technology and workforce development on Semiconductors in Mexico
1:00 pm	Prof. Vijaykrishnan Narayanan	CSE and EE, Penn State U.	Designing emerging computing systems with ferroelectric devices
1:30 pm	Prof. João Antonio Martino	University of São Paulo, Brazil	MOSFET evolution from planar to 3D structure

Sayeef Salahuddin

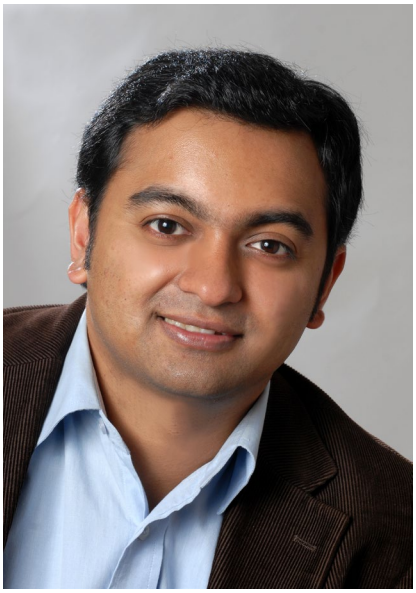
Sayeef Salahuddin is the TSMC Distinguished professor of Electrical Engineering and Computer Sciences at the University of California Berkeley. Salahuddin received his B.Sc. in Electrical and Electronic Engineering from BUET (Bangladesh University of Engineering and Technology) in 2003 and PhD in Electrical and Computer Engineering from Purdue University in 2007. He joined the faculty of Electrical Engineering and Computer Science at University of California, Berkeley in 2008.

His work has focused on conceptualization and exploration of novel device physics for low power electronic and spintronic devices. Salahuddin has championed the concept of using 'interacting systems' for switching, showing fundamental advantage of such systems over the conventional devices in terms of power dissipation. This led to the discovery of Negative Capacitance Transistors that allows for sub kT/q subthreshold operation in transistors.

Salahuddin has received the Presidential Early Career Award for Scientist and Engineers (PECASE), the highest honor bestowed by the US Government on early career scientist and engineers. Salahuddin also received a number of other awards including the NSF CAREER award, the IEEE Nanotechnology Early Career Award, the Young Investigator Awards from the Air Force Office of Scientific Research (AFOSR) and the Army Research Office (ARO) and best paper awards from IEEE Transactions on VLSI Systems and from the VLSI-TSA conference. In 2012, Applied Physics Letters (APL) highlighted two of his papers among 50 most notable papers among all areas published in APL within 2009-2012. Salahuddin also received the George E Smith Award from the IEEE Electron Devices Society.

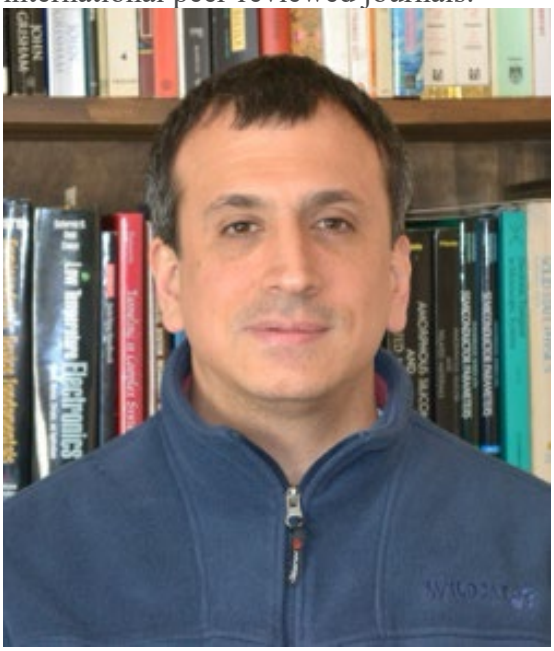
Salahuddin is a co-director of the Berkeley Device Modeling Center and Berkeley Center for Negative Capacitance Transistors. He served on the editorial board of IEEE Electron Devices Letters (2013-16) and was the chair the IEEE Electron Devices Society committee on Nanotechnology (2014-16).

Salahuddin is a fellow of the IEEE and the APS.



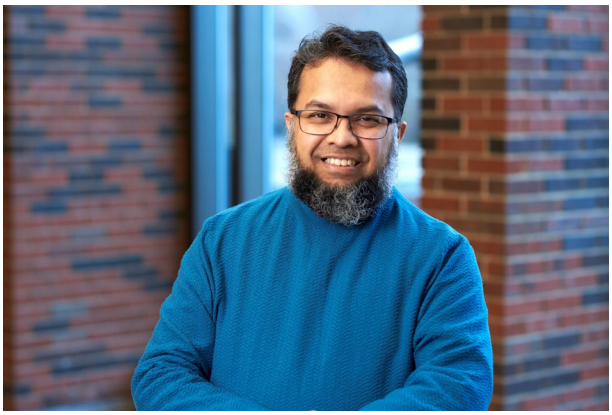
Felix Palumbo

I am Principal Device Eng at Allegro Microsystems, and full professor at UTN in Buenos Aires. I have received the MSc. (2000) and the PhD (2005) both in physics from the University of Buenos Aires, Argentina. I am an active researcher in the field of semiconductor device physics and reliability, transport in mesoscopic systems and oxide-semiconductor interfaces with experience in the academy and industry. From 2006 to 2023, I have been research staff of the National Council of Science and Technology (CONICET), well embedded within international research collaboration. In the 2015 IEEE-IRPS edition, I have been invited to present a review talk on CMOS Reliability, and in the 2019-IRPS edition I was awarded with the best paper recognition. Concerning projects management and research grants, I participated in several international funded research projects. My interest for applied science prompted me to start research collaborations with companies such as IBM-Fishkill-USA, Tower Jazz-Israel, SOITEC-France, and I am also a frequent scientific visitor of academic institutions as IMM-CNR-Italy, the IMEP-LAHC Lab.-Minatec site, Grenoble-France, the Autonomous University of Barcelona -Spain, and the Israel Institute of Technology-Technion. Regarding the teaching activities, I am full professor at National Technological University (UTN) in Buenos Aires, Argentina, where the supervision of PhD students and managerial responsibilities are relevant issues among my activities. My actual research interests are in the field of reliability of innovative devices, BCD technology and radiation effects on semiconductors devices. I am reviewer of several scientific journals, author of two review articles, and of about forty scientific and technical papers published on international peer-reviewed journals.



Muhammad Mustafa Hussain

Muhammad Mustafa Hussain (Professor, ECE, Purdue University) pioneered vFabLab for equitable access to semiconductor training. His initiatives, including Chips Changing the World, STARS, VICTORS, Berkeley Engineering Innovates, Winter Camp on Microelectronics Gadget, IEEE EDS Workshop on Sustainable Electronics, Podcast with EDS Luminaries, Nano-scholarship, Semiconductor Fabrication 101, etc. have aided over 30,000 learners. His research spanning UC Berkeley, KAUST, SEMATECH and Texas Instruments focuses on futuristic electronics. With 22 supervised PhD graduates, 425+ research papers, and patents, he is a Fellow of IEEE, APS, and IoP. Awarded the CES 2020 Best Innovation Award, his research is frequently celebrated in global media.



Gilson Wirth

Gilson Wirth received the B.S.E.E and M.Sc. degrees from the Universidade Federal do Rio Grande do Sul, Brazil, in 1990 and 1994, respectively. In 1999 he received the Dr.-Ing. degree in Electrical Engineering from the University of Dortmund, Dortmund, Germany.

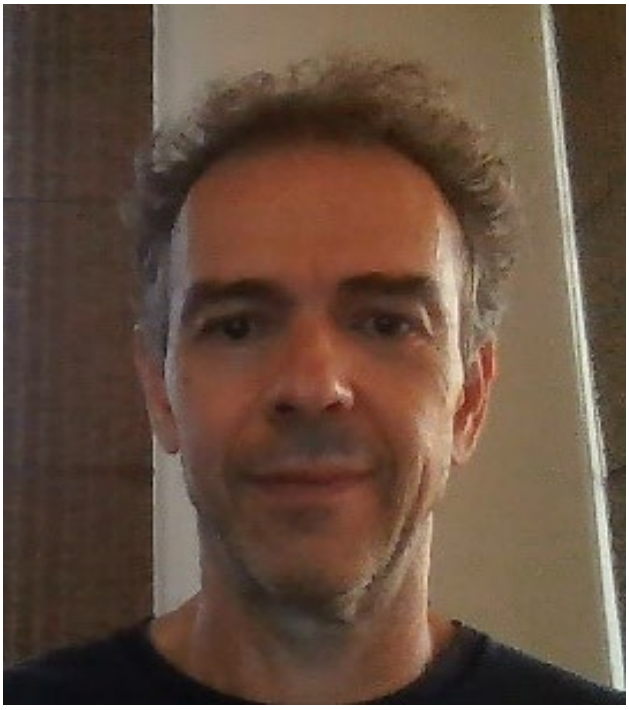
He is currently a professor at the Electrical Eng. Depart. at Univ. Federal do Rio Grande do Sul - UFRGS (since January 2007).

From July 2002 to December 2006 he was professor and head of the Computer Engineering Department, Univ. Estadual do Rio Grande do Sul - UERGS.

His current research work focuses on modeling and electrical simulation of charge trapping in the context of Bias Temperature Instability (BTI), Low-Frequency Noise (1/f and RTN) and Hot Carrier Degradation (HCD).

He has also worked on ionizing radiation effects (TID and SET/SEU) on semiconductor devices. He focuses on collaborative work with academia and industry. He has stablished successful collaborative work with different companies and research groups in Europe, North and South America, and China. Has signed NDA with the following companies: Intel, Texas Instruments, NXP Semiconductors and Infineon Technologies.

He is currently a Distinguished Lecturer of the IEEE Electron Devices Society. He also was a distinguished lecturer of the IEEE Circuits and Systems Society (term 2010-2011).
An updated list of publications may be found at http://lattes.cnpq.br/1745194055679908
Or https://www.webofscience.com/wos/author/record/319677
Or https://www.scopus.com/authid/detail.uri?authorId=8700162500



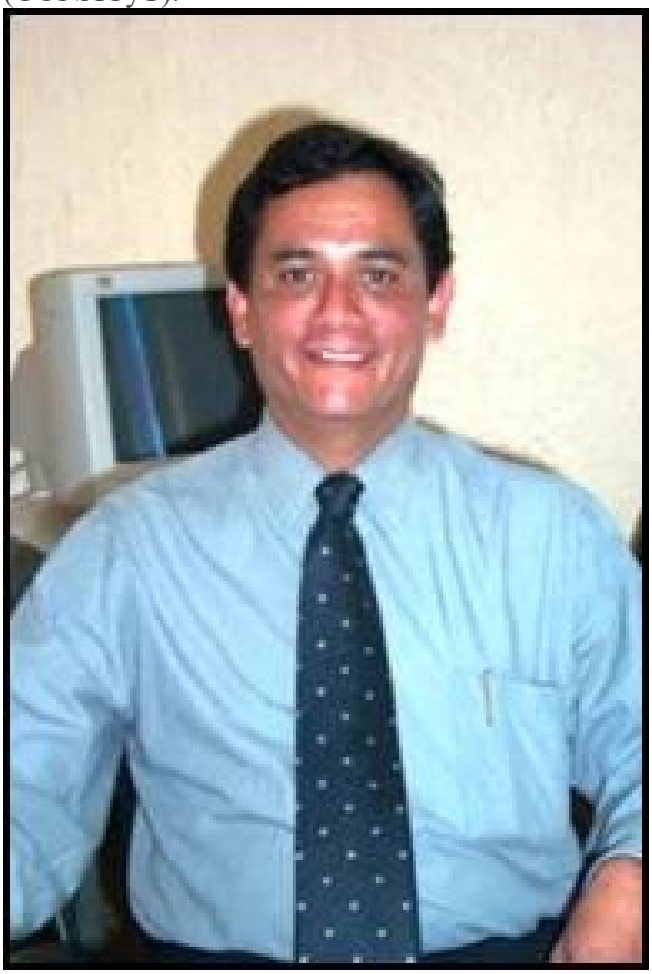
Katy Crist

Katy Crist joined TEL in 2002 and has steadily advanced, gaining expertise across various business domains including product, field services, support, media development, training, global communications, corporate marketing and workforce development. As a versatile and adept team leader, she thrives on navigating the dynamic tech landscape. Currently, as Senior Manager of Strategic Alliances and Partnerships at Tokyo Electron Limited (TEL), a key player in semiconductors and flat panel display equipment, Katy oversees the growth and implementation of academia and military partnerships, workforce development initiatives, and public relations efforts. With nearly two decades of experience, she excels in communicating across all organizational levels, ensuring successful program execution from inception to fruition. Additionally, Katy contributes her expertise as a board member of the SEMI Foundation for the last 5 years.

Dr. Edmundo A. Gutiérrez-D.

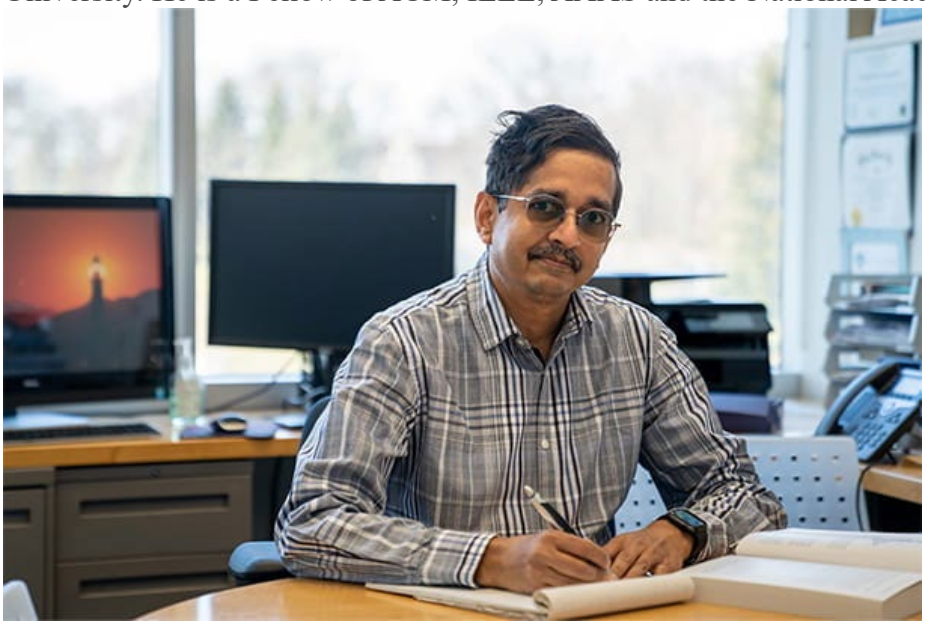
Dr. Edmundo A. Gutiérrez-D. got his PhD in 1993 from the Catholic University of Leuven, Belgium with the thesis entitled “Electrical performance of submicron CMOS technologies from 300 K to 4.2 K”. From 1989 to 1993, while working for his PhD, served as a research assistant at the Interuniversity Microelectronics Center (IMEC) in Leuven, Belgium. In 1996 was guest Professor at Simon Fraser University, Vancouver, Canada. In 1996 spent two months as an invited lecturer at the Sao Paulo University, Brazil. In 2000 acted as Design Manager of the Motorola Mexico Center for Semiconductor Technology. In 2002 was invited lecturer at the Technical University of Vienna, Austria. In 2005 joined the Intel Mexico Research Center as technical Director. Currently he holds a Professor position at the National Institute for Astrophysics, Optics and Electronics (INAOE), in Puebla, Mexico. Prof. Gutiérrez-D. is an IEEE senior member since 2008.

Professor Gutiérrez-D. has published over 100 scientific publications and conferences in the field of semiconductor device physics, has supervised 5 M.Sc. and 10 Ph.D. thesis, and is author of the book “Low Temperature Electronics, Physics, Devices, Circuits and Applications” published by Academic Press in 2000. Prof. Gutiérrez-D. is member of the Mexico National System of Researchers and technical reviewer for the Mexico National Council for Science and Technology (CONACyT).



Vijaykrishnan Narayanan

Vijaykrishnan Narayanan is an Evan Pugh University Professor and Robert Noll A. Chair Professor of Computer Science and Engineering and Electrical Engineering at The Pennsylvania State University. He is a Fellow of ACM, IEEE, AAAS and the National Academy of Inventors.



João Martino

Joao Antonio Martino received master (1984) and PhD (1988) degrees in microelectronics from University of Sao Paulo, Brazil. He was a postdoctoral researcher in silicon-on-insulator (SOI) devices and technology in Imec, Belgium. He is currently a full professor and the head of SOI group at University of Sao Paulo. His expertise is in electrical characterization, simulation and modeling of SOI devices in wide temperature range. He is also interested in the SOI-CMOS fabrication process, multiple-gate devices (FinFET), 1T-DRAM, Tunnel-FET and radiation effects. He has authored or coauthored of more than 400 technical journal papers and conference presentation and author/editor of 5 books. He is senior member and distinguished lecturer of the IEEE Electron Device Society (EDS). He is chair of IEEE/EDS South Brazil chapter and vice-chair of SRC IEEE/EDS R9.